IN THE CLAIMS

The current claims follow. For claims not marked as amended in this response, any difference in the claims below and the previous state of the claims is unintentional and in the nature of a typographical error.

1. (Currently Amended) A demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of said orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M=2^N$, said demodulator comprising:

a Logic 00 input detector capable of comparing sequential, non-overlapping pairs of said M binary bits of said serially received orthogonal modulation codes to a Logic 00 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur;

a summation circuit comprising S accumulators;

a Logic 00 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 00 switch array is capable of coupling an output of said Logic 00 input detector to a first input of a Kth one of said S accumulators;

a storage array capable of storing S code masks associated with said S orthogonal modulation codes, wherein each of said S code masks comprises M/2 code mask bits and each of said M/2 code mask bits is associated with a corresponding one of said sequential pairs of said M binary bits in one of said orthogonal modulation codes; and

control circuitry capable of synchronously applying the M/2 code mask bits in a Kth one of said S code masks in said storage array as a switch control signal to said Kth switch in said Logic 00 switch array such that a Logic 1 code mask bit in said Kth code mask closes said Kth switch in said Logic 00 switch array whenever said Logic 00 input detector is comparing a sequential pair of said M binary bits equal to 00, thereby connecting the [+1,+1] output signals of said Logic 00 input detector to said first input of said Kth accumulator.

2. (Currently Amended) The demodulator as set forth in Claim 1 further comprising:

a Logic 01 input detector capable of comparing sequential, non-overlapping pairs of said M binary bits of said serially received orthogonal modulation codes to a Logic 01 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and

a Logic 01 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 01 switch array is capable of coupling an output of said Logic 01 input detector to a second input of said Kth accumulator, wherein said control circuitry is capable of synchronously applying the M/2 code mask bits in said Kth code mask in said storage array as a switch control signal to said Kth switch in said Logic 01 switch array such that a Logic 1 code mask bit in said Kth code mask closes said Kth switch in said Logic 01 switch array whenever said Logic 01 input detector is comparing a sequential pair of said M binary bits equal to 01, thereby connecting the [+1,+1] output signals of said Logic 01 input detector to said second input of said Kth accumulator.

3. (Currently Amended) The demodulator as set forth in Claim 2 further comprising:

a Logic 10 input detector capable of comparing sequential, non-overlapping pairs of said M binary bits of said serially received orthogonal modulation codes to a Logic 10 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and

a Logic 10 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 10 switch array is capable of coupling an output of said Logic 10 input detector to a third input of said Kth accumulator, wherein said control circuitry is capable of synchronously applying the M/2 code mask bits in said Kth code mask in said storage array as a switch control signal to said Kth switch in said Logic 10 switch array such that a Logic 1 code mask bit in said Kth code mask closes said Kth switch in said Logic 10 switch array whenever said Logic 10 input detector is comparing a sequential pair of said M binary bits equal to 10, thereby connecting the [+1,+1] output signals of said Logic 10 input detector to said third input of said Kth accumulator.

4. (Currently Amended) The demodulator as set forth in Claim 3 further comprising:

a Logic 11 input detector capable of comparing sequential, non-overlapping pairs of said M binary bits of said serially received orthogonal modulation codes to a Logic 11 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and

a Logic 11 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 11 switch array is capable of coupling an output of said Logic 11 input detector to a fourth input of said Kth accumulator, wherein said control circuitry is capable of synchronously applying

the M/2 code mask bits in said Kth code mask in said storage array as a switch control signal to said Kth switch in said Logic 11 switch array such that a Logic 1 code mask bit in said Kth code mask closes said Kth switch in said Logic 11 switch array whenever said Logic 11 input detector is comparing a sequential pair of said M binary bits equal to 11, thereby connecting the [+1,+1] output signals of said Logic 11 input detector to said fourth input of said Kth accumulator.

5. (Original) The demodulator as set forth in Claim 4 further comprising a code selection circuit capable of reading a sum value from each said S accumulators and identifying an accumulator containing a maximum sum value.

6. (Original) The demodulator as set forth in Claim 5 wherein said code selection circuit outputs one of 2^M N-bit data symbols corresponding to said identified accumulator containing said maximum value.

7. (Original) The demodulator as set forth in Claim 6 wherein N=6 and M= 2^N=64.

8. (Original) The demodulator as set forth in Claim 7 wherein S=64.

9. (Original) The demodulator as set forth in Claim 8 wherein said orthogonal modulation codes are Walsh codes.

10. (Currently Amended) A code division multiple access (CDMA) wireless network comprising a plurality of base transceiver stations capable of communicating with access terminals located in a coverage area of said wireless network, wherein a first one of said plurality of base transceiver stations comprises:

a demodulator for demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of said orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M=2^N$, said demodulator comprising:

a Logic 00 input detector capable of comparing sequential, non-overlapping pairs of said M binary bits of said serially received orthogonal modulation codes to a Logic 00 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur;

a summation circuit comprising S accumulators;

a Logic 00 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 00 switch array is capable of coupling an output of said Logic 00 input detector to a first input of a Kth one of said S accumulators;

a storage array capable of storing S code masks associated with said S orthogonal modulation codes, wherein each of said S code masks comprises M/2 code mask bits and each of said M/2 code mask bits is associated with a corresponding one of said sequential pairs of said M binary bits in one of said orthogonal modulation codes; and

control circuitry capable of synchronously applying the M/2 code mask bits in a Kth one of said S code masks in said storage array as a switch control signal to said Kth switch in said Logic 00 switch array such that a Logic 1 code mask bit in said Kth code mask closes said Kth switch in said Logic 00 switch array whenever said Logic 00 input detector is comparing a sequential pair of said M binary bits equal to 00, thereby connecting the [+1,+1] output signals of said Logic 00 input detector to said first input of said Kth accumulator

11. (Currently Amended) The CDMA wireless network as set forth in Claim 10 further comprising:

a Logic 01 input detector capable of comparing sequential, non-overlapping pairs of said M binary bits of said serially received orthogonal modulation codes to a Logic 01 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and

a Logic 01 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 01 switch array is capable of coupling an output of said Logic 01 input detector to a second input of said Kth accumulator, wherein said control circuitry is capable of synchronously applying the M/2 code mask bits in said Kth code mask in said storage array as a switch control signal to said Kth switch in said Logic 01 switch array such that a Logic 1 code mask bit in said Kth code mask closes said Kth switch in said Logic 01 switch array whenever said Logic 01 input detector is comparing a sequential pair of said M binary bits equal to 01, thereby connecting the [+1,+1] output signals of said Logic 01 input detector to said second input of said Kth accumulator.

12. (Currently Amended) The CDMA wireless network as set forth in Claim 11 further comprising:

a Logic 10 input detector capable of comparing sequential, non-overlapping pairs of said M binary bits of said serially received orthogonal modulation codes to a Logic 10 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and

a Logic 10 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 10 switch array is capable of coupling an output of said Logic 10 input detector to a third input of said Kth accumulator, wherein said control circuitry is capable of synchronously applying the M/2 code mask bits in said Kth code mask in said storage array as a switch control signal to said Kth switch in said Logic 10 switch array such that a Logic 1 code mask bit in said Kth code mask closes said Kth switch in said Logic10 switch array whenever said Logic 10 input detector is comparing a sequential pair of said M binary bits equal to 10, thereby connecting the [+1,+1] output signals of said Logic 10 input detector to said third input of said Kth accumulator.

13. (Currently Amended) The CDMA wireless network as set forth in Claim12 further comprising:

a Logic11 input detector capable of comparing sequential, non-overlapping pairs of said M binary bits of said serially received orthogonal modulation codes to a Logic 11 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and

a Logic 11 switch array comprising S switches, wherein a Kth one of said S switches in said Logic 11 switch array is capable of coupling an output of said Logic 11 input detector to a fourth input of said Kth accumulator, wherein said control circuitry is capable of synchronously applying the M/2 code mask bits in said Kth code mask in said storage array as a switch control signal to said Kth switch in said Logic 11 switch array such that a Logic 1 code mask bit in said Kth code mask closes said Kth switch in said Logic 11 switch array whenever said Logic 11 input detector is comparing a sequential pair of said M binary bits equal to 11, thereby connecting the [+1,+1] output signals of said Logic 11 input detector to said fourth input of said Kth accumulator.

14. (Original) The CDMA wireless network as set forth in Claim 13 further comprising a code selection circuit capable of reading a sum value from each said S accumulators and identifying an accumulator containing a maximum sum value.

15. (Original) The CDMA wireless network as set forth in Claim 14 wherein said code selection circuit outputs one of 2^M N-bit data symbols corresponding to said identified accumulator containing said maximum value.

16. (Original) The CDMA wireless network as set forth in Claim15 wherein N=6 and M= 2^N=64.

17. (Original) The CDMA wireless network as set forth in Claim 16 wherein S=64.

18. (Original) The CDMA wireless network as set forth in Claim17 wherein said orthogonal modulation codes are Walsh codes.

19. (Currently Amended) For use in a base station of a wireless network capable of communicating with mobile stations located in a coverage area of the wireless network, a method of demodulating a set of S possible orthogonal modulation codes received serially as binary data, wherein each of the orthogonal modulation codes comprises M binary bits representing an N-bit data symbol and wherein $M=2^N$, the method comprising the steps of:

in a Logic 00 input detector, comparing sequential, non-overlapping pairs of the M binary bits of the serially received orthogonal modulation codes to a Logic 00 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur;

retrieving from a storage array the Kth one of S code masks associated with the S orthogonal modulation codes, wherein each of the S code masks comprises M/2 code mask bits and each of the M/2 code mask bits is associated with a corresponding one of the sequential pairs of the M binary bits in one of the orthogonal modulation codes; and

synchronously applying the M/2 code mask bits of the Kth S code mask as a switch control signal to the Kth switch in a Logic 00 switch array comprising S switches, wherein the Kth switch in the Logic00 switch array is capable of coupling an output of the Logic00 input detector to a first

input of a Kth one of S accumulators, and wherein a Logic 1 code mask bit in the Kth code mask closes the Kth switch in the Logic 00 switch array whenever the Logic00 input detector is comparing a sequential pair of the M binary bits equal to 00, thereby connecting the [+1,+1] output signals of the Logic 00 input detector to the first input of the Kth accumulator.

20. (Currently Amended) The method as set forth in Claim 19 further comprising the steps of:

in a Logic 01 input detector, comparing sequential, non-overlapping pairs of the M binary bits of the serially received orthogonal modulation codes to a Logic 01 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and

synchronously applying the M/2 code mask bits of the Kth S code mask as a switch control signal to the Kth switch in a Logic 01 switch array comprising S switches, wherein the Kth switch in the Logic 01 switch array is capable of coupling an output of the Logic 01 input detector to a second input of the Kth accumulator, and wherein a Logic 1 code mask bit in the Kth code mask closes the Kth switch in the Logic01 switch array whenever the Logic 01 input detector is comparing a sequential pair of the M binary bits equal to 01, thereby connecting the [+1,+1] output signals of the Logic01 input detector to the second input of the Kth accumulator.

21. (Currently Amended) The method as set forth in Claim20 further comprising the steps of:

in a Logic10 input detector, comparing sequential, non-overlapping pairs of the M binary bits of the serially received orthogonal modulation codes to a Logic10 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and

synchronously applying the M/2 code mask bits of the Kth S code mask as a switch control signal to the Kth switch in a Logic10 switch array comprising S switches, wherein the Kth switch in the Logic 10 switch array is capable of coupling an output of the Logic10 input detector to a third input of the Kth accumulator, and wherein a Logic1 code mask bit in the Kth code mask closes the Kth switch in the Logic10 switch array whenever the Logic 10 input detector is comparing a sequential pair of the M binary bits equal to 10, thereby connecting the [+1,+1] output signals of the Logic 10 input detector to the third input of the Kth accumulator.

22. (Currently Amended) The method as set forth in Claim21 further comprising the steps of:

in a Logic 11 input detector, comparing sequential, non-overlapping pairs of the M binary bits of the serially received orthogonal modulation codes to a Logic 11 value and outputting a [+1,+1] signal if a match occurs and outputting a [-1,-1] signal if a match does not occur; and

synchronously applying the M/2 code mask bits of the Kth S code mask as a switch control signal to the Kth switch in a Logic 11 switch array comprising Sswitches, wherein the Kth switch in

the Logic 11 switch array is capable of coupling an output of the Logic11 input detector to a fourth input of the Kth accumulator, and wherein a Logic 1 code mask bit in the Kth code mask closes the Kth switch in the Logic 11 switch array whenever the Logic11 input detector is comparing a sequential pair of the M binary bits equal to 11, thereby connecting the [+1,+1] output signals of the Logic 11 input detector to the fourth input of the Kth accumulator.